20 self-aligned, anti-via interconnects in the manufacture of the integrated circuit device wherein said anti-reflective coating layer is a polishing stop.

Please cancel Claim 13.

REMARKS

Examiner J. Maldonado is thanked for the thorough examination and search of the subject Patent Application. Claims 1 and 9 have been amended. Claims 4 and 13 have been canceled.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 1-3 rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,693,568 to Liu et al is requested based on the following remarks.

Applicant agrees that Liu teaches a method to form interconnects in an integrated circuit device. However, Liu does not teach the step of partially etching through the metal layer to form vias using a timed etch as taught in Applicant's amended

Claim 1 as shown above. Claim 1 has been amended to include the limitation of a timed etch as taught in original Claim 4. Claim 4 has been canceled. Since the limitation of a timed etch is not taught by Liu, Amended Claim 1 is patentably distinct from Liu. Further, dependent Claims 2-3 represent patentably distinct further limitations on Claim 1 and should be in condition for allowance.

Reconsideration of Claims 1-3 rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,693,568 to Liu et al is requested based on the above remarks.

Reconsideration of Claims 4-23 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,693,568 to Liu et al in view of U.S. Patent 6,080,660 to Wang et al is requested based on the following remarks.

Applicant agrees that Liu teaches a method to form interconnects in an integrated circuit device. However, Liu does not teach the step of etching though the anti-reflective coating layer and the second metal layer to form vias using a timed etch as in Applicant's Amended Claim 9. Amended Claim 9 adds the limitation of a timed etch as in original Claim 13. Claim 13 has

therefore been canceled. Wang does mention the use of a timed etch. However, it is not obvious to one skilled in the art to combine the teachings of Wang with Liu as proposed by the Examiner for two reasons. First, the time etch of Wang is performed on a conductive layer 22 through an opening 26 in a dielectric layer 23 (Fig. 2C). This is not analogous to the timed etch performed by the Applicant where no dielectric layer is formed overlying the conductive layer 70, 66, 62, and 58, prior to the timed etching (Fig. 5). Second, the timed etch of Wang generates a slanted topography (Fig. 2C and column 4, lines 26-37). This slanted topography would be destructive in Applicant's invention for a via coupling to an overlying metal interconnect as shown by the Applicant in Fig. 9. Therefore, the timed etch taught by Wang is not compatible with the teachings of the Applicant. Therefore, it is not obvious for one skilled in the art to combine the teachings of Liu with Wang to create the method taught by the Applicant in Amended Claim 9. Amended Claim 9 should be in condition for allowance. Further Claims 10-12 and 14-17 represent patentably distinct further limitations on Claim 9 and should also be in condition for allowance.

In regards to Claim 18, Liu does not teach the use of an anti-reflective coating layer comprising titanium nitride.

Further, although Wang describes a titanium/titanium nitride layer 24 overlying the conductor 22, it is not obvious to one skilled in the art to combine the teachings of Wang with Liu as proposed by the Examiner for two reasons. First, the titanium/titanium nitride layer 24 of Wang is deposited prior to the dielectric layer 23 (Fig. 2C). Further, since the dielectric layer is etched prior to the etching of the titanium/titanium nitride layer 24, the sides of the conductive layer 22 are not exposed to the etching process. Second, a part of the titanium/titanium nitride layer 24 is left overlying the conductive layer 22 where not exposed by the dielectric layer 23. Therefore, the titanium/titanium nitride layer 24 taught by Wang is not analogous with the teachings of the Applicant. Therefore, it is not obvious for one skilled in the art to combine the teachings of Liu with Wang to create the method taught by the Applicant in Amended Claim 9. Claim 18 should be in condition for allowance. Further Claims 19-23 represent patentably distinct further limitations on Claim 18 and should also be in condition for allowance.

Reconsideration of Claims 4-23 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,693,568 to Liu

et al in view of U.S. Patent 6,080,660 to Wang et al is requested based on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner J. Maldonado not find that the Claims are now Allowable that he call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

Douglas R. Schnabel, Reg. No. 47,927

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend Claim 1 as follows:

1. (Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a metal layer overlying said semiconductor substrate;

etching through said metal layer to form connective lines;

thereafter etching partially through said metal layer to form vias using a timed etch;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device.

Please cancel Claim 4.

Please amend Claim 9 as follows:

9. (Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing a second metal layer overlying said first metal layer;

depositing an anti-reflective coating layer comprising titanium nitride (TiN) overlying said second metal layer;

etching through said anti-reflective coating layer, said second metal layer, and said first metal layer to form connective lines;

thereafter etching through said anti-reflective coating layer and said second metal layer to form vias <u>using a timed etch</u>;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said

self-aligned, anti-via interconnects in the manufacture of the integrated circuit device wherein said anti-reflective coating layer is a polishing stop.

Please cancel Claim 13.